CSCE430/830
Computer Architecture
Fall 2007

Instructor: Dr. Hong Jiang
jiang@cse.unl.edu
Cse.unl.edu/~jiang/cse430
472-6747

Department of Computer Science & Engineering
University of Nebraska-Lincoln

Classroom: 109 Avery Hall; Time: 11:30am-12:20pm, M. W.F.
Office Hour: 10:30am-11:20pm, M. W.F.; Office: 268 Avery
TA for Design Project: Mr. Zhipeng Ouyang, zouyang@cse.unl.edu
Office Hours: 1:00pm-5:00pm, Monday; Building 501, Rm 5
TA for grading: Mr. Lin Lin, lilin@cse.unl.edu
Office Hours: 4:00pm-6:00pm, Tuesday; 13A Avery Hall
Course Syllabus

• **Description:**
  430/830. Computer Architecture (3 cr) Prereq: CSCE 230, 230L, 310 (Coreq: Math 380 or EE 410) or permission. Addresses the architecture of single-processor (Von Neumann or SISD) computer systems, with an emphasis on performance estimation. Topics: Memory Systems, including technologies, hierarchies, interleaving, virtual memory, cache implementation; Communications & I/O, including bus architectures, arbitration, I/O processors, DMA; Processor Architectures, including RISC & CISC approaches, pipelining in a single-processor system. Credit not applicable toward graduate degree in computer science.

• **Course Schedule:**
  An overview and tentative (and approximate) schedule of the course is listed below:

<table>
<thead>
<tr>
<th>Main Topics to Be Covered</th>
<th>Readings Required</th>
<th>Lecture Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fundamentals of Computer Design</td>
<td>Chapter 1: 1.1-1.9</td>
<td>2-3 lectures</td>
</tr>
<tr>
<td>Instruction Set Principles</td>
<td>Appendix B: 2.1-2.7</td>
<td>3-4 lectures</td>
</tr>
<tr>
<td>Instruction-Level Parallelism, Its Dynamic Exploitation &amp; Limitations</td>
<td>Selected Sections in Chapters 2 &amp; 3</td>
<td>12-14 lectures</td>
</tr>
<tr>
<td>Memory Hierarchy Design: Cache, Virtual Memory, Virtual Machines</td>
<td>Appendix C &amp; Chapter 5: 5.1-5.6</td>
<td>10-12 lectures</td>
</tr>
<tr>
<td>Storage Systems &amp; Networks</td>
<td>Chapters 6 &amp; Appendix E (selected)</td>
<td>8-10 lectures</td>
</tr>
<tr>
<td>Others: prereq test; exams;</td>
<td>As needed</td>
<td>1 lecture each</td>
</tr>
</tbody>
</table>
Course Syllabus (cont.)

Grading Policy:

• **Pre-requisite exam** will be given on the Monday of the third week, with preparation materials provided during the 1st two weeks.

• **2 equally weighted exams** will be given at around the sixth and twelfth week respectively.

• **Design project** will be required in lieu of the final exam—a semester-long team project—with details to be announced.

• **4-5 homework assignments** will be given. Each is due in class on its specified due date. Late work is penalized 20% per day. Once solutions are published, late work cannot be accepted for credit.

• While collaboration on homework is permitted, blatant copying will not be tolerated. Violators, if caught, will subject to penalties ranging from a zero for the homework assignment in question to an F grade for the course, depending on the severity of the violation.

• **Final Grade** will be generated according to the weight associated with each component listed below:

  - Pre-requisite Test: 5%
  - Homework Assignment: 25%
  - Exam 1: 20%
  - Exam 2: 20%
  - Design Project: 30%